Χαρίδημος Θ. Βέργος
Καθηγητής
Πανεπιστήμιο Πατρών
Τμήμα Μηχανικών Η/Υ & Πληροφορικής

Βιογραφικό σημείωμα

Οκτώβριος 2015

Περιεχόμενα

Γενικά στοιχεία

Ονοματεπώνυμο :	Χαρίδημος Βέργος
Όνομα Πατρός :	Θεοφάνης
Ημερομηνία γέννησης :	30 Αυγούστου 1968
Οικογενειακή κατάσταση :	Έγγαμος, 3 παιδιά
Διεύθυνση κατοικίας :	Ευρώτα 17, 264 42, Πάτρα
Τηλέφωνο επικοινωνίας :	+30 2610 996924
FAX :	+30 2610 991909
e–mail :	vergos@ceid.upatras.gr
Web Page :	http://pc–vlsi18.ceid.upatras.gr

Τίτλοι σπουδών

- First Certificate in English, Cambridge University, Φεβρουάριος 1982, Grade : B.
- Απολυτήριο Γενικού Λυκείου, Πρότυπο Λύκειο Πατρών, Ιούνιος 1986, Βαθμός : Άριστα, $19\frac{10}{12}$.
- Certificate of Proficiency in English, Cambridge University, Φεβρουάριος 1988, Grade : C.
- Δίπλωμα Μηχανικού Η/Υ & Πληροφορικής, Οκτώβριος 1991, Βαθμός : Άριστα, $8\frac{54}{100}$.
  Η προπτυχιακή διπλωματική μου εργασία με τίτλο ¨Σχεδιασμός και Ανάπτυξη ενός Συστήματος Οπτικής Αναγνώρισης Χαρακτήρων¨, έφτασε μέχρι και το στάδιο του βιομηχανικού πρωτοτύπου. Μεταξύ άλλων, η εργασία αυτή περιελάμβανε :
  - έλεγχο μηχανολογικού εξοπλισμού κίνησης ενός βραχίονα στον οποίο ήταν στερεωμένο ένα Charged–Coupled Device (CCD),
  - τοπική αποθήκευση των δεδομένων του CCD,
  - μεταφορά της πληροφορίας μέσω interrupt–driven DMA σε έναν προσωπικό υπολογιστή και
  - ανάπτυξη πρότυπου λογισμικού για την επεξεργασία της πληροφορίας.
- Διδακτορικό Δίπλωμα, Πανεπιστήμιο Πατρών, Φεβρουάριος 1996.
  Το θέμα της διδακτορικής μου διατριβής ήταν ¨Σχεδιασμός Συστήματος Κρυφής Μνήμης με Ικανότητα Ανοχής Ελαττωμάτων¨ (http://thesis.ekt.gr/thesisBookReader/id/6773). Στη διατριβή αυτή προτάθηκαν τρεις μέθοδοι για την αντιμετώπιση των συνεπειών από ελαττώματα που συμβαίνουν κατά την κατασκευή ή κατά τη λειτουργία ολοκληρωμένων κυκλωμάτων που περιλαμβάνουν ένα ή περισσότερα επίπεδα κρυφής μνήμης. Επίσης παρουσιάστηκε ένα στατιστικό μοντέλο πρόβλεψης της αύξησης της γραμμής παραγωγής ολοκληρωμένων κυκλωμάτων μικροεπεξεργαστών μέσω της ανοχής ελαττωμάτων των ενσωματωμένων κρυφών μνημών.

Επαγγελματική πορεία

1988–1991 : Εργαστήριο Ψηφιακών Συστημάτων (ΕΨΗΣ), Ερευνητικό Ακαδημαϊκό Ινστιτούτο Τεχνολογίας Υπολογιστών (ΕΑΙΤΥ).
Κύρια απασχόλησή μου ήταν η προμήθεια ολοκληρωμένων κυκλωμάτων, επιστημονικών οργάνων και εργαλείων λογισμικού για ηλεκτρονικό σχεδιασμό (E–CAD). Επίσης ήμουν ο εισηγητής των προδιαγραφών για μεγάλο μέρος του εξοπλισμού που αποκτήθηκε στα πλαίσια των προγραμμάτων ΜΟΠ–10 και ΜΟΠ–11.

1990–1991 : Ανάπτυξη μιας βάσης δεδομένων για την Πνευμονολογική Κλινική του Κέντρου Νοσημάτων Θώρακος – Νοσοκομείο Πατρών ¨ Άγιος Ανδρέας¨.
Η βάση αυτή χρησιμοποιείται για το μητρώο ασθενών της κλινικής και την εξαγωγή στατιστικών ερευνητικών δεδομένων.

11/1991 – 2/1996 : Υποψήφιος διδάκτορας του ΤΜΗΥΠ, υπότροφος του ΕΑΙΤΥ και Ειδικός Μεταπτυχιακός Υπότροφος (ΕΜΥ) του Πανεπιστημίου Πατρών (υποτροφία από κονδύλια της Επιτροπής Ερευνών).

5/1996–11/1997 : Εκπόνηση της στρατιωτικής θητείας μου, με ειδικότητα Ειδικού Επιστήμονα (Προγραμματιστής Η/Υ).
Ήμουν υπεύθυνος της Μηχανογράφησης του Κέντρου Εκπαιδεύσεως Τεχνικού και κατά τη διάρκεια της θητείας μου επιτεύχθηκε για πρώτη φορά η δικτύωση των διαφόρων μονάδων του Κέντρου.

1/1998–9/1998 : ATMEL ΑΕΒΕΕ, τμήμα Ανάπτυξης Ολοκληρωμένων για Επικοινωνιακές και Πολυμεσικές εφαρμογές, Σχεδιαστής υλικού.
Συμμετείχα στην ανάπτυξη δύο ολοκληρωμένων κυκλωμάτων :

- ◇ Το πρώτο από αυτά (VirtualNet, 802.11b Baseband and MAC) αποτελεί το πρώτο ολοκληρωμένο – σύστημα (System on a Chip–SOC) το οποίο σχεδιάστηκε εξ' ολοκλήρου στην Ελλάδα, και το πρώτο παγκοσμίως που υλοποίησε πλήρως το MAC επίπεδο για ασύρματα δίκτυα, σύμφωνα με το IEEE 802.11b standard. Σε συνέχεια αυτού, παρουσιάστηκαν παρόμοια ολοκληρωμένα με διαφορετικό προσαρμογέα, ολοκληρωμένα που πραγματοποιούν γεφύρωση μεταξύ ενσύρματων και ασύρματων υποδικτύων (wireless to Ethernet bridging), κλπ.
- ◇ Το δεύτερο ολοκληρωμένο ήταν ένας πολυπλέκτης / αποπλέκτης για ενσύρματα και οπτικά δίκτυα. Σκοπός του ήταν να πολυπλέκει / αποπλέκει δεδομένα τεσσάρων πηγών, κάθε μία των 155 Mbps (ATM payload), σε / από πακέτα του SONET OC–12 (SDH STM–4).

9/1998–4/2003 : Λέκτορας επί θητεία, Πανεπιστήμιο Πατρών, ΤΜΗΥΠ (ΦΕΚ διορισμού 171/17–9–1998, τεύχος Ν.Π.Δ.Δ).

4/2003–1/2007 : Επίκουρος Καθηγητής επί θητεία, Πανεπιστήμιο Πατρών, ΤΜΗΥΠ (ΦΕΚ διορισμού 90/24–4–2003, τεύχος Ν.Π.Δ.Δ).

1/2007–3/2009 : Μόνιμος Επίκουρος Καθηγητής, Πανεπιστήμιο Πατρών, ΤΜΗΥΠ (ΦΕΚ μονιμοποίησης 44/25–1–2007, τεύχος Γ').

3/2009–1/2014 : Αναπληρωτής Καθηγητής, Πανεπιστήμιο Πατρών, ΤΜΗΥΠ, Τομέας Υλικού και Αρχιτεκτονικής των Υπολογιστών (ΦΕΚ διορισμού 172/5–3–2009, τεύχος Γ').

2/2014–σήμερα : Καθηγητής, Πανεπιστήμιο Πατρών, ΤΜΗΥΠ, Τομέας Υλικού και Αρχιτεκτονικής των Υπολογιστών (ΦΕΚ διορισμού 112/30–1–2014, τεύχος Γ').

Διδακτικό έργο και λοιπή εκπαιδευτική δραστηριότητα

α. Μη αυτόνομο διδακτικό έργο

Κατά τη διάρκεια της εργασίας μου στο ΕΨΗΣ και της εκπόνησης της διδακτορικής μου διατριβής, διεξήγαγα φροντιστήρια και εργαστηριακά μαθήματα του ΤΜΗΥΠ, τα οποία συνοψίζονται στον ακόλουθο πίνακα :

Ονομασία	**Είδος**	**Εξάμηνο Προγράμματος Σπουδών**	**Ακαδημαϊκά Έτη**	**Μέσος Αριθμός Φοιτητών που Παρακολούθησε**
Βασικά Ηλεκτρονικά	Εργαστήριο	Β	1991–1992 1992–1993	120
Αρχιτεκτονική Η/Υ	Φροντιστήριο	Γ	1993–1994 1994–1995 1995–1996	120
	Εργαστήριο	Δ	1993–1994 1995–1996	120
Ψηφιακά Ηλεκτρονικά	Εργαστήριο	Δ	1991–1992 1992–1993	120
Μικροεπεξεργαστές	Εργαστήριο	Ε	1990–1991	120
Εισαγωγή στο Ε–CAD	Εργαστηριακό μάθημα	Ζ	1989–1990 1990–1991	80
Εισαγωγή στο Σχεδιασμό VLSI	Εργαστήριο	Η	1990–1991	40
Διασύνδεση Μικροϋπολογιστικών Συστημάτων	Εργαστηριακό μάθημα	Η	1990–1991	10
Έλεγχος Ορθής Λειτουργίας VLSI Κυκλωμάτων	Φροντιστήριο	Θ	1993–1994	12
	Εργαστήριο	Θ	1993–1994	12

Κατόπιν του αιφνιδίου θανάτου του Επίκουρου Καθηγητή κ. Αν. Βέργη και σχετικής εισηγήσεως της Συνέλευσης του Τομέα Υλικού και Αρχιτεκτονικής του ΤΜΗΥΠ (επισυνάπτεται στο παράρτημα Α) δίδαξα υπό την επίβλεψη του Καθηγητή κ. Αλεξίου το Μάθημα ¨Συστήματα Υπολογιστών ΙΙ¨ του Β΄ εξαμήνου σπουδών του ΤΜΗΥΠ κατά το ακαδημαϊκό έτος 1995–1996.

β. Αυτόνομο διδακτικό έργο

Μετά την εκλογή μου σε θέση ΔΕΠ του ΤΜΗΥΠ έχω διδάξει / διδάσκω τα μαθήματα που συνοψίζονται στον ακόλουθο πίνακα :

Ονομασία	Είδος	Εξάμηνο Προγράμματος Σπουδών	Ακαδημαϊκά Έτη	Μέσος Αριθμός Φοιτητών που Παρακολούθησε
Ψηφιακά Ηλεκτρονικά	Μάθημα	Δ	1997–1998	180
Εισαγωγή στα Συστήματα Υπολογιστών	Μάθημα	Α	1998–1999 έως και 2003–2004	220
Εργαστήριο Συστημάτων Υπολογιστών	Εργαστήριο	Β	1998–1999 έως και 2003–2004	200
Σχεδιασμός Συστημάτων Ειδικού Σκοπού †	Μάθημα	Ελεύθερης επιλογής χειμερινού εξαμήνου	1999–2000 έως και 2015–2016	22
Σχεδίαση Συστημάτων με Χρήση Υπολογιστών (Ε–CAD)‡	Εργαστηριακό μάθημα	Βασικό επιλογής εαρινού εξαμήνου	1999–2000 έως και 2015–2016	11
Λογική Σχεδίαση Ι	Μάθημα	Α	2007–2008 έως και 2015–2016	275
Λογική Σχεδίαση ΙΙ	Μάθημα	Β	2004–2005 έως και 2015–2016	225
Υπολογιστικά Συστήματα Υψηλής Αξιοπιστίας	Μεταπτυχιακό μάθημα	Χειμερινό	1999–2000 έως και 2015–2016	4

Από το ακαδημαϊκό έτος 2004-2005, διδάσκω επίσης ως Συνεργαζόμενο Εκπαιδευτικό Προσωπικό του Ελληνικού Ανοικτού Πανεπιστημίου, στη Θεματική ενότητα ¨Ψηφιακά Συστήματα¨, στα πλαίσια του προπτυχιακού προγράμματος σπουδών Πληροφορικής.

γ. Ανάπτυξη/επικαιροποίηση εκπαιδευτικού υλικού και εισαγωγή νέων μαθημάτων

γ.1. Συγγραφικό έργο

◇ *Σχεδίαση Συστημάτων με Χρήση Υπολογιστών*, Πανεπιστημιακές Παραδόσεις, 1η έκδοση 1998, 2η έκδοση 2004.

◇ *Εισαγωγή στα Συστήματα Υπολογιστών*, Πανεπιστημιακές Παραδόσεις, 1η έκδοση 2001, 2η έκδοση 2003, 3η έκδοση 2004.
Ηλεκτρονικό αντίγραφο αυτού του συγγράμματος διανεμήθηκε μαζί με το τεύχος Αυγούστου 2010, στους αναγνώστες του ευρέως κυκλοφορίας περιοδικού πληροφορικής PC magazine.

†Κατά το ακαδημαϊκό έτος 2013–2014 το μάθημα Σχεδιασμός Συστημάτων Ειδικού Σκοπού παρακολούθησαν και φοιτητές του Τμήματος Ηλεκτρολόγων Μηχανικών και Τεχνολογίας Υπολογιστών, κατόπιν επιλογής τους.

‡Κατά τα ακαδημαϊκά έτη 1999–2000 έως και 2004–2005 το μάθημα Σχεδίαση Συστημάτων με Χρήση Υπολογιστών (Ε–CAD) και το αντίστοιχο εργαστήριο παρακολούθησαν και φοιτητές του Τμήματος Ηλεκτρολόγων Μηχανικών και Τεχνολογίας Υπολογιστών, κατόπιν επιλογής τους.

◇ *Εγχειρίδιο Χρήσης AT91*, Πανεπιστημιακές Παραδόσεις, 1η έκδοση 2009.

◇ *Εγχειρίδιο Ασκήσεων Εργαστηρίου Συμβολικής Γλώσσας (Assembly)*, 1η έκδοση 2008.

◇ *Εγχειρίδιο Ασκήσεων Εργαστηρίου Μικροεπεξεργαστών*, 1η έκδοση 2008, 2η έκδοση 2009.

γ.2. Ανάπτυξη νέου και επικαιροποίηση παλαιού εκπαιδευτικού υλικού

◇ *Ανάπτυξη της νέας πλατφόρμας AT91 για τη διεξαγωγή εργαστηριακών ασκήσεων.*
Η πλατφόρμα αυτή φιλοξενεί τα εργαστήρια προγραμματισμού σε συμβολική γλώσσα και διασύνδεσης και προγραμματισμού μικροεπεξεργαστή για επικοινωνία με περιφερειακές συσκευές. Για τη νέα αυτή πλατφόρμα ήμουν υπεύθυνος ανάπτυξης όλου του υποστηρικτικού υλικού (εγχειρίδια χρήσης, εκφωνήσεις ασκήσεων, υποδειγματικές λύσεις, κλπ.).
Η πλατφόρμα AT91 χρησιμοποιήθηκε για πρώτη φορά το ακαδημαϊκό έτος 2008–2009 για τα εργαστήρια συμβολικής γλώσσας και το ακαδημαϊκό έτος 2009–2010 στα εργαστήρια μικροεπεξεργαστών, ενώ έχει αναπτυχθεί και εκπαιδευτικό υλικό για την υποστήριξη εργαστηρίων αρχιτεκτονικής.

◇ *Επικαιροποίηση της ύλης του μαθήματος "Σχεδίαση Συστημάτων με Χρήση Υπολογιστών (E-CAD)" και των αντίστοιχων εργαστηριακών ασκήσεων και υποδομών.*
Εισήχθησαν σύγχρονοι τρόποι περιγραφής κυκλωμάτων (FSMs, HDLs) και οι πλέον διαδεδομένοι τρόποι γρήγορης πρωτοτυποποίησης των σχεδιασμών με τη χρήση προγραμματιζόμενων ολοκληρωμένων, (Programmable Logic Devices, FPGAs).

γ.3. Εισαγωγή νέων μαθημάτων

◇ *Σχεδιασμός Συστημάτων Ειδικού Σκοπού (προπτυχιακό)* και

◇ *Υπολογιστικά Συστήματα Υψηλής Αξιοπιστίας (μεταπτυχιακό).*

δ. Επίβλεψη διπλωματικών εργασιών - Συνεπίβλεψη διδακτορικών διατριβών

Έχω επιβλέψει τις ακόλουθες διπλωματικές εργασίες για το προπτυχιακό πρόγραμμα σπουδών του ΤΜΗΥΠ :

1. Ανάπτυξη firmware για ασύρματο δίκτυο σύμφωνα με το πρωτόκολλο 802.11 της IEEE, Χριστοδούλου Θεοδώρα, 2000.
2. Επεξεργαστικό στοιχείο RNS, Κουρέτας Ιωάννης, 2001.
3. Διασύνδεση ενός επεξεργαστή για ασύρματα δίκτυα με το δίαυλο PCI, Γκρίμπας Δημήτριος, 2001.
4. Υλοποίηση σε VLSI και βελτιστοποίηση ενός αυτοδιδασκόμενου ισοσταθμιστή για συστήματα επικοινωνίας τρίτης γενιάς, Τζεράνης Γεώργιος, 2001, σε συνεργασία με τον κ. Μπερμπερίδη, Καθηγητή του ΤΜΗΥΠ.
5. Ανάπτυξη αρχιτεκτονικής για ένα αυτοδιδασκόμενο ισοσταθμιστή για συστήματα επικοινωνίας τρίτης γενιάς, Γιαννόπουλος Θεόδωρος, 2001, σε συνεργασία με τον κ. Μπερμπερίδη, Καθηγητή του ΤΜΗΥΠ.
6. Ποιότητα υπηρεσιών σε ασύρματα τοπικά δίκτυα, Νεοφύτου Στέλιος, 2003.
7. KoVer : ένα εργαλείο παραγωγής εναλλακτικών αρχιτεκτονικών για αριθμητική υπολοίπων, Κωστάρας Νικόλαος, 2005.
Από αυτή τη διπλωματική εργασία προέκυψε η εργασία W.5 του καταλόγου δημοσιευμάτων.

8. Διασύνδεση ενός GPS receiver με προσωπικό υπολογιστή, Μαριδάκης Νικόλαος, 2006.
9. Κώδικες Reed–Solomon : Μελέτη και ανάπτυξη γεννήτορα του κυκλώματος κωδικοποίησης, Καγιάς Γεώργιος, 2006.
10. Ανάπτυξη πλακέτας για την υποστήριξη των εργαστηρίων E–CAD, Τσιάτουρας Δημήτριος, 2006.
11. Ανάπτυξη ηλεκτρονικού μαγνητοφώνου σε προγραμματιζόμενη λογική, Σπηλιόπουλος Ηλίας, 2007.
12. Ανάπτυξη νέας πλακέτας για τα εργαστήρια αρχιτεκτονικής υπολογιστών, Κωστόπουλος Φώτιος, 2007.
13. Εξέταση εναλλακτικών αρχιτεκτονικών κυκλωμάτων αριθμητικής υπολοίπου για υλοποίηση σε FPGAs, Σπύρου Αναστασία, 2007.
14. Επεξεργαστής LEON : Υλοποίηση σε FPGA και ανάπτυξη διασυνδετικών σχεδιασμών με γνωστά πρότυπα, Κουρή Ιωάννα, 2008.
15. Ανάπτυξη master–slave cores για δίαυλο I2C, Ντάσιος Ευάγγελος, 2008.
16. Αθροιστές BCD. Βιβλιογραφική μελέτη των εναλλακτικών αρχιτεκτονικών και συγκριτική υλοποίησή τους σε VLSI, Δημακοπούλου Παρασκευή–Ιωάννα, 2009.
17. Βιβλιογραφική μελέτη και υλοποίηση σε υλικό των κρυπτογραφικών συναρτήσεων κατακερματισμού MD5 και SHA-1, Μαυρόπουλος Μιχαήλ, 2010.
18. Αλγόριθμοι κρυπτογράφησης IDEA και IDEA new. Βιβλιογραφική μελέτη και υλοποίηση σε VLSI, Κουτσιουμάρης Νικόλαος, 2010.
19. Αλγόριθμος κρυπτογραφίας RSA. Βιβλιογραφική μελέτη και εναλλακτικές υλοποιήσεις σε VLSI, Κασιώλας Βασίλειος, 2010.
20. Σχεδιασμός και υλοποίηση κρυπτογραφικού συστήματος βασισμένο στο πρότυπο AES με υποστήριξη πολλαπλών κλειδιών, Μπεχτσούδης Ανέστης, 2010.
21. Ανάπτυξη βιβλιοθηκών αριθμητικών σχεδιασμών σε τεχνολογία Quantum–Dot Cellular Automata, Γιάννου Ολυμπία, 2011.
    Από αυτή τη διπλωματική αυτή εργασία, προέκυψε το δημοσίευμα υπ΄ αριθμόν C.46 του καταλόγου.
22. Εξέταση εναλλακτικών VLSI αρχιτεκτονικών για αθροιστές επανεισαγόμενου κρατουμένου 128 δυαδικών ψηφίων και η χρήση τους σε μονάδες κινητής υποδιαστολής, Μπαρούτης Νικόλαος, 2011.
23. Ανάπτυξη αριθμητικών κυκλωμάτων σε τεχνολογία Quantum–Dot Cellular Automata, Θάνος Αλέξιος, 2011.
    Από αυτή τη διπλωματική αυτή εργασία, προέκυψε το δημοσίευμα υπ΄ αριθμόν C.50 του καταλόγου.
24. Ανάπτυξη βιβλιοθήκης αριθμητικών κυκλωμάτων σε πλεονάζουσες αναπαραστάσεις, Κωνσταντίνος Γκουγκουλιάς, 2012.
25. Υδατογράφηση σχεδιασμών υψηλού επιπέδου (IP Watermarking at the behavioral level), Αναστάσιος Μπίκος, 2012.
    Από αυτή τη διπλωματική αυτή εργασία, προέκυψε το δημοσίευμα υπ΄ αριθμόν C.51 του καταλόγου.
26. Υλοποίηση ψηφιακού (FIR) φίλτρου χρησιμοποιώντας κλασσική δυαδική αναπαράσταση και αναπαράσταση στο σύστημα υπολοίπων, Γρηγόριος Αδαμόπουλος, 2012.
27. Συγκριτές απόστασης Hamming, Αγγελική Αναστασίου, 2013.
    Από αυτή τη διπλωματική αυτή εργασία, προέκυψε το δημοσίευμα υπ΄ αριθμόν J.29 του καταλόγου.
28. Υλοποίηση ενός 2D–DCT core, Παναγιώτης Χρηστάκος, 2013.
    Η διπλωματική αυτή διεξήχθη σε συνεργασία με την εταιρεία NanotropIC.

29. Υλοποίηση του παιχνιδιού pong για δύο παίκτες σε ΦΠΓΑ, Διαλυνάς Νικόλαος, 2014.
30. Ανάπτυξη HDL γεννητόρων για αρχιτεκτονικές εντοπισμού των δύο ελαχίστων / μεγίστων καθώς και πλήρους ταξινόμησης, Σκαρτσίλας Νικόλαος, 2014.
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   Η κ. Χριστοδούλου εργάζεται σήμερα στο Υπουργείο Παιδείας.
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   Από τη διπλωματική αυτή εργασία, προέκυψαν τα δημοσιεύματα υπ΄ αριθμόν J.17 και C.28 του καταλόγου.
   Ο κ. Αδαμίδης αφού εργάστηκε στην εταιρεία ATMEL ως σχεδιαστής κυκλωμάτων, σήμερα εργάζεται στο IC Design Center της Texas Instruments, στη Νίκαια της Γαλλίας.
3. Ανάπτυξη πλατφόρμας για την εκπόνηση εργαστηριακών ασκήσεων, Ν. Κωστάρας, Ιούνιος 2008.
   Ο κ. Κωστάρας αφού εργάστηκε στην εταιρεία ATMEL στην ανάπτυξη ενσωματωμένου λογισμικού, και ακολούθως στις εταιρείες Nanoradio, στο Κίιστα της Σουηδίας, AFK Sistema (Sitronics) και Altera, στο Λονδίνο, σήμερα εργάζεται στην Sepura, ως senior low–level–software engineer.
4. Κυκλώματα ύψωσης στο τετράγωνο για αριθμητικά συστήματα υπολοίπων, Αν. Σπύρου, Ιούνιος 2009.
   Από τη διπλωματική αυτή προέκυψαν οι εργασίες υπ΄ αριθμόν J.24 και C.36 του καταλόγου δημοσιευμάτων.
   Η κ. Σπύρου εργάζεται ως μηχανικός λογισμικού για χρηματοοικονομικές εφαρμογές, στην εταιρεία Accenture.
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   Η διπλωματική αυτή εργασία αποτέλεσε τη βάση για τις εργασίες J.19, J.22, C.34 και C.35 του καταλόγου δημοσιευμάτων.

Υπήρξα συνεπιβλέπων των διδακτορικών διατριβών :

1. Τεχνικές ελέγχου ορθής λειτουργίας με έμφαση στη χαμηλή κατανάλωση ισχύος, Μάτσιεϊ Μπέλλος, 2007.
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2. Αποδοτικά κυκλώματα για το Αριθμητικό Σύστημα Υπολοίπων, Ευάγγελος Βασσάλος, 2013.
   Από τη διατριβή αυτή προέκυψαν τα δημοσιεύματα υπ΄ αριθμόν J.25, I.1, C.39, C.43, C.44, C.45 και C.47 του καταλόγου.

Ερευνητικό έργο

α. Κατάλογος Δημοσιευμάτων

α.1. Διατριβές

D.1. Σχεδιασμός Συστήματος Κρυφής Μνήμης με Ικανότητα Ανοχής Ελαττωμάτων, Χ. Βέργος, ΤΜΗΥΠ, Πανεπιστήμιο Πατρών, 1996.

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‡Μια εμπλουτισμένη μορφή της εργασίας B.2 κρίθηκε κατ' αρχάς δημοσιεύσιμη στο περιοδικό Journal of Systems Architecture. (Η σχετική επιστολή επισυνάπτεται στο παράρτημα Β του παρόντος). Ωστόσο λόγω των στρατιωτικών μου υποχρεώσεων στάθηκε αδύνατο να γίνουν οι απαιτούμενες από τους κριτές αλλαγές σε εύλογο χρονικό διάστημα.

*Η εργασία C.1 έχει αρκετές φορές χρησιμοποιηθεί σαν εργασία βάσης για κάποιες από τις εξαμηνιαίες εργασίες (projects) που θα πρέπει να κάνουν οι μεταπτυχιακοί φοιτητές στα πλαίσια του μαθήματος "Fault Tolerant Computing", στο Πανεπιστήμιο του Wisconsin, Madison

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C.29. New Architectures for Modulo $2^n - 1$ Adders, G. Dimitrakopoulos, D. G. Nikolos, H. T. Vergos, D. Nikolos and C. Efstathiou, 12$^{\text{th}}$ IEEE International Conference on Electronics, Circuits and Systems, (ICECS 2005), Grammath, Tunisia, December 11–14, 2005.

C.30. Novel Modulo $2^n + 1$ Multipliers, H. T. Vergos and C. Efstathiou, 9$^{\text{th}}$ Euromicro Conference on Digital System Design, (DSD '06), Cavtat near Dubrovnik, Croatia, August 30–September 1, 2006, pp. 168–175.

C.31. Efficient Modulo $2^k + 1$ Squarers, H. T. Vergos and C. Efstathiou, XXI Conference on Design of Circuits and Integrated Systems (DCIS 2006), Barcelona, Spain, November 22–24, 2006.

C.32. An Efficient BIST Scheme for Non–Restoring Array Dividers, H. T. Vergos, 10$^{\text{th}}$ Euromicro Conference on Digital System Design, (DSD '07), Lübeck, Germany, August 29–31, 2007, pp. 664–667.

C.33. Fast Modulo $2^n + 1$ Adder Architectures, H. T. Vergos, XXII Conference on Design of Circuits and Integrated Systems, (DCIS 2007), Sevilla, Spain, November 21–23, 2007, pp. 476–481.

C.34. Efficient Modulo $2^n + 1$ Multi–Operand Adders, H. T. Vergos, D. Bakalis and C. Efstathiou, 15$^{\text{th}}$ IEEE International Conference on Electronics, Circuits and Systems (ICECS 2008), Malta, August 31–September 3, 2008, pp. 694–697.

C.35. On the Use of Diminished–1 Adders for Weighted Modulo $2^n + 1$ Arithmetic Components, H. T. Vergos and D. Bakalis, 11$^{\text{th}}$ Euromicro Conference on Digital System Design : Architectures, Methods and Tools (DSD 2008), Parma, Italy, September 3–5, 2008, pp. 752–759.

C.36. Efficient Architectures for Modulo $2^n - 1$ Squarers, A. Spyrou, D. Bakalis and H. T. Vergos, 16$^{\text{th}}$ International Conference on Digital Signal Processing (DSP 2009), Santorini, Greece, July 5–7, 2009.

C.37. Novel Modulo $2^n + 1$ Subtractors, E. Vassalos, D. Bakalis and H. T. Vergos, 16$^{\text{th}}$ International Conference on Digital Signal Processing (DSP 2009), Santorini, Greece, July 5–7, 2009.

C.38. A Family of Area–Time Efficient Modulo $2^n + 1$ Adders, H. T. Vergos, IEEE Annual Symposium on VLSI (ISVLSI 2010), Kefallonia, Greece, July 5–7, 2010, pp. 442–443.

C.39. SUT–RNS Forward and Reverse Converters, E. Vassalos, D. Bakalis and H. T. Vergos, IEEE Annual Symposium on VLSI (ISVLSI 2010), Kefallonia, Greece, July 5–7, 2010, pp. 11–17.

C.40. Area Efficient Multi–Moduli Squarers for RNS, D. Bakalis and H. T. Vergos, 13$^{\text{th}}$ Euromicro Conference on Digital System Design : Architectures, Methods and Tools (DSD 2010), Lille, France, September 1–3, 2010, pp. 408–411.

C.41. Diminished–1 Modulo $2^n + 1$ Multiply–Add Circuits, D. Bakalis and H. T. Vergos, XXV Conference on Design of Circuits and Integrated Systems (DCIS 2010), Lanzarotte, Spain, November 17–19, 2010, pp. 289–294.

C.42. Area–Time Efficient Multi–Moduli Adder Design, H. T. Vergos and D. Bakalis, XXV Conference on Design of Circuits and Integrated Systems (DCIS 2010), Lanzarotte, Spain, November 17–19, 2010, pp. 295–300.

C.43. On the Use of Double LSB and Signed-LSB Encodings for RNS, E. Vassalos, D. Bakalis and H. T. Vergos, 17$^{\text{th}}$ International Conference on Digital Signal Processing, Corfu, Greece, July 6–8, 2011.

C.44. Modulo $2^n + 1$ Arithmetic Units with Embedded Diminished-to-Normal Conversion, E. Vassalos, D. Bakalis and H. T. Vergos, 14$^{\text{th}}$ Euromicro Conference on Digital System Design : Architectures, Methods and Tools (DSD 2011), Oulu, Finland, August 31 - September 2, 2011, pp. 468–475.

C.45. Configurable Booth–Encoded Modulo $2^n \pm 1$ Multipliers[†], E. Vassalos, D. Bakalis and H. T. Vergos, 8$^{\text{th}}$Conference on Ph.D. Research in Microelectronics & Electronics (PRIME 2012), Aachen, Germany, June 12–15 2012, pp. 107–110.

C.46. Squarers in QCA Nanotechnology, H. T. Vergos, O. Giannou and D. Bakalis, 12$^{\text{th}}$ IEEE International Conference on Nanotechnology (IEEE-NANO), Birmingham, UK, August 20–23, 2012, pp. 689–694.

C.47. SUT-RNS Residue-to-Binary Converters Design, E. Vassalos, D. Bakalis and H. T. Vergos, 15$^{\text{th}}$ Euromicro Conference on Digital System Design : Architectures, Methods and Tools (DSD 2012), Cesme, Turkey, September 5-8, 2012, pp. 65–72.

C.48. Reverse Converters for RNSs with Diminished-One Encoded Channels, E. Vassalos, D. Bakalis and H. T. Vergos, IEEE Region 8 Eurocon Conference, Zagreb, Croatia, July 1-4, 2013, pp. 1798-1805.

C.49. RNS Assisted Image Filtering and Edge Detection, E. Vassalos, D. Bakalis and H. T. Vergos, 18$^{\text{th}}$ IEEE International Conference On Digital Signal Processing (DSP 2013), Santorini, Greece, July 1-3, 2013, pp. 1–6.

C.50. Fast Parallel–Prefix Ling–Carry Adders in QCA Nanotechnology, A. Thanos and H. T. Vergos, IEEE International Conference on Electronics, Circuits, and Systems (ICECS 2013), Abu Dhabi, UAE, December 8-11, 2013, pp. 565–568.

C.51. Easily Verified IP Watermarking, A. Bikos and H. T. Vergos, Design & Technology of Integrated Systems at Nanoscale Era (DTIS 2014), Santorini, Greece, May 6–8, 2014, pp. 8–9.

◇ Η κρίση όλων των παραπάνω εργασιών εξαιρουμένης της C.46, έγινε επί του πλήρους κειμένου τους.

◇ Τα πρακτικά των παραπάνω συνεδρίων, πλην των C.6, C.8, C.12, C,13, C.17, C.20, C.25, C.31, C.33, C.41 και C.42 εκδίδονται από ACM / IEEE Societies.

α.7. Δημοσιεύματα σε συνεδρίες (Workshops)

W.1. Reconfigurable CPU Cache Memory Design : Fault Tolerance and Performance Evaluation, D. Nikolos, H. T. Vergos and P. Mitsiadis, 1$^{\text{st}}$ IEEE International On–Line Testing Workshop, July 4–6, 1995, Nice, France, pp. 8–10.

W.2. On The Testability Of Low–Power Optimized Circuits, M. Perakis, H. T. Vergos and D. Nikolos, 2$^{\text{nd}}$ IEEE International On–Line Testing Workshop, July 8–10, 1996, Biarritz, France, pp. 234–235.

W.3. On–Line Path Delay Fault Testing of Omega MINs, M. Bellos, E. Kalligeros, D. Nikolos and H. T. Vergos, 5$^{\text{th}}$ IEEE International On–Line Testing Workshop, July 5–7, 1999, Rhodes, Greece, pp. 133–137.

W.4. A Formal Test Set for RNS Adders and an Efficient Low Power BIST Scheme, H. T. Vergos, D. Nikolos, M. Bellos and C. Efstathiou, 2$^{\text{nd}}$ IEEE Latin American Testing Workshop (LATW 2001), February 11–14, 2001, Cancun, Mexico, pp. 242–247.

W.5. KoVer : A Sophisticated Residue Arithmetic Core Generator, N. Kostaras and H. T. Vergos, 16$^{\text{th}}$ IEEE International Workshop on Rapid System Prototyping (RSP 2005), June 8–10, Montreal, Canada, pp. 261–263.

◇ Η κρίση όλων των παραπάνω εργασιών έγινε επί του πλήρους κειμένου τους.

[†]Στην εργασία αυτή απονεμήθηκε το Silver Leaf Certificate (παρατίθεται στο Παράρτημα Γ.) γιατί κατετάγη βάσει της βαθμολογίας των κριτών ανάμεσα στο 10% και 20% των καλυτέρων εργασιών που υπεβλήθησαν στο συνέδριο.

α.8. Τεχνικές εκθέσεις (Reports)

R.1. Fault Tolerant CPU Cache Memory Design, H. T. Vergos and D. Nikolos, Computer Technology Institute Technical Report No. 94.12.59, December 1994.

R.2. Performance Recovery in Faulty Direct–Mapped Caches via the Use of a Very Small Fully Associative Spare Cache, H. T. Vergos and D. Nikolos, Computer Technology Institute Technical Report No. 94.12.60, December 1994.

R.3. Reconfigurable CPU Cache Memory Design : Fault Tolerance and Performance Evaluation, H. T. Vergos, D. Nikolos and P. Mitsiadis, Computer Technology Institute Technical Report No. 95.1.5, January 1995.

R.4. On the Yield of VLSI Processors with On–Chip CPU Cache, D. Nikolos and H. T. Vergos, Computer Technology Institute Technical Report No. 95.12.42, December 1995.

R.5. Path Delay Fault Testable Modified Booth Multipliers, E. Kalligeros, H. T. Vergos, D. Nikolos, Y. Tsiatouhas and Th. Haniotakis, Computer Technology Institute Technical Report No. 99.07.01, July 1999.

R.6. Easily Path Delay Fault Testable Non–Restoring Cellular Array Dividers, G. Sidiropoulos, H. T. Vergos and D. Nikolos, Computer Technology Institute Technical Report No. 99.07.05, July 1999.

R.7. Low Power BIST for Wallace–Tree Based Fast Multipliers, D. Bakalis, E. Kalligeros, D. Nikolos, H. T. Vergos and G. Alexiou, Computer Technology Institute Technical Report No. 99.09.07, September 1999.

R.8. Modified Booth 1's Complement and Modulo $2^n - 1$ Multipliers, C. Efstathiou and H. T. Vergos, Computer Technology Institute Technical Report No. 2000.09.03, September 2000.

R.9. Diminished-1 Modulo $2^n + 1$ Adder Design, H. T. Vergos, C. Efstathiou and D. Nikolos, Computer Technology Institute Technical Report No. 2001.02.02, February 2001.

β. Ερευνητικές κατευθύνσεις

Οι εργασίες του προηγηθέντος καταλόγου αντικατοπτρίζουν έρευνα στα ακόλουθα αντικείμενα :

- ◇ Αρχιτεκτονικές κρυφών μνημών για την ελάττωση των συνεπειών που επιφέρουν οι κατασκευαστικές ατέλειες στην απόδοση του συστήματος μνήμης και στην απόδοση της γραμμής κατασκευής. Στα πλαίσια έρευνας αυτού του αντικειμένου αναπτύχθηκε και ένα μοντέλο πρόβλεψης της απόδοσης της γραμμής παραγωγής ολοκληρωμένων επεξεργαστών με ενσωματωμένες κρυφές μνήμες ενός ή δύο επιπέδων (Εργασίες D.1, J.1 και J.2, B.1 και B.2, C.1 και C.2, W.1 και R.1 έως R. 4).
- ◇ Έλεγχος ορθής λειτουργίας αριθμητικών κυκλωμάτων κάτω από κλασσικά ή ενδελεχή μοντέλα σφαλμάτων καθυστέρησης και ανάπτυξη αρχιτεκτονικών για ενσωματωμένο έλεγχο (Εργασίες J.4, J.9, B.3, C.3 έως C.8, C.10, C.15, C.22, C.24, W.3 και W.4, R.5 και R.6).
- ◇ Το πρόβλημα της κατανάλωσης σε αντιπαράθεση με αυτό της ελεγξιμότητας και ανάπτυξη αποτελεσματικών αρχιτεκτονικών ενσωματωμένου ελέγχου χαμηλής κατανάλωσης για αριθμητικά κυκλώματα (Εργασίες J.5 και J.6, C.9, C.11 και C.32, W.2 και R.7).
- ◇ Ανάπτυξη εργαλείων λογισμικού για την αυτόματη παραγωγή αριθμητικών κυκλωμάτων ή / και ενσωματωμένων δομών ελέγχου της ορθής τους λειτουργίας καθώς και εργαλείων εκτίμησης της απόδοσης κρυφών μνημών πολλών βαθμίδων (Εργασίες J.16, B.4, C.13 και W.5).

- ◇ Εξέταση της καταλληλότητας προταθέντων αρχιτεκτονικών στις νέας γενιάς τεχνολογίες υλοποίησης (Εργασία C.19).
- ◇ Γρήγορη ανάπτυξη συστημάτων μέσω ολοκλήρωσης ετερογενών σχεδιαστικών κομματιών και συσχεδίασης υλικού-λογισμικού (Εργασία C.12).
- ◇ Ανάπτυξη αποδοτικών αρχιτεκτονικών για κυκλώματα αριθμητικής υπολοίπου (Εργασίες J.3, J.7, J.8, J.10 έως J.15, J.17 έως J.28, I.1, C.14, C.16 έως C.18, C.20, C.21, C.23, C.25 έως C.31, C.33 έως C.45, C.47 έως C.49, R.8 και R.9).
- ◇ Ανάπτυξη αριθμητικών κυκλωμάτων για νανοτεχνολογίες υλοποίησης (Εργασίες C.46 και C.50).
- ◇ Υδατογράφηση σχεδιαστικών πυρήνων (Εργασία C.51).

γ. Αναφορές από άλλους ερευνητές

Η βιβλιογραφική βάση Scholar Google καταγράφει 947 συνολικές αναφορές στο ερευνητικό μου έργο συμπεριλαμβανομένων αυτοαναφορών και αναφορών από συσυγγραφείς, 573 εκ των οποίων εντός της τελευταίας πενταετίας. Επίσης καταγράφει h-index ίσο με 15 και i10-index ίσο με 21.

Η βιβλιογραφική βάση Scopus καταγράφει 576 συνολικές αναφορές σε 66 μόνο εκ των εργασιών του ερευνητικού μου έργου συμπεριλαμβανομένων αυτοαναφορών και αναφορών από συσυγγραφείς, 419 εκ των οποίων είναι ετεροαναφορές. Επίσης, καταγράφει h-index ίσο με 9.

Στο παράρτημα Δ του παρόντος παρατίθεται αναλυτικός κατάλογος επιβεβαιωμένων αναφορών στο ερευνητικό μου έργο, ο οποίος καταγράφει 778 ετεροαναφορές από 407 εργασίες τρίτων και 108 αναφορές από συσσυγγραφείς σε 23 εργασίες τους.

δ. Κρίση επιστημονικών εργασιών

Έχω χρησιμοποιηθεί ως κριτής επιστημονικών εργασιών στα παρακάτω περιοδικά και συνέδρια :

- ◇ IEEE Transactions on Computers,
- ◇ IEEE Transactions on Computers - Special Issues on Computer Arithmetic 2009 & 2011,
- ◇ IEEE Transactions on Circuits and Systems I,
- ◇ IEEE Transactions on Circuits and Systems II,
- ◇ IEEE Transactions on Very Large Scale Integration (VLSI) Systems,
- ◇ IEEE Transactions on Signal Processing,
- ◇ IEEE Signal Processing Letters,
- ◇ IET Computers and Digital Techniques (IEE Proceedings - Computers and Digital Techniques),
- ◇ IET Circuits, Devices and Systems (IEE Proceedings - Circuits, Devices and Systems),
- ◇ Integration, the VLSI Journal,
- ◇ Journal of Electronic Testing : Theory and Applications,
- ◇ International Journal of Electronics,
- ◇ International Journal of Computer Mathematics,
- ◇ International Journal of Computer Systems Science and Engineering,
- ◇ Theoretical Computer Science,
- ◇ Computers and Mathematics with Applications,
- ◇ Information Processing Letters,

- ◇ Journal of Applied Mathematics,
- ◇ Journal of Signal Processing Systems,
- ◇ Journal of Circuits, Systems and Computers,
- ◇ ASP Journal of Low Power Electronics (JoLPE),
- ◇ Advances in Electrical Engineering,
- ◇ Design, Automation and Test in Europe Conferences (DATE), 2000 & 2003,
- ◇ XIV, XV, XVII & XVIII Design of Circuits and Integrated Systems Conferences (DCIS),
- ◇ 3rd (EDCC-3), 8th (EDCC-8) & 10th (EDCC-10) European Dependable Computing Conference, 1999, 2010 & 2014,
- ◇ 6th, 7th, 8th, 9th, 10th, 11th, 15th, 16th & 17th IEEE International Conferences on Electronics, Circuits and Systems, (ICECS 1999, 2000, 2001, 2002, 2003, 2008, 2009 & 2010),
- ◇ 9th Asian Test Symposium, 2000,
- ◇ 13th, 14th & 15th IEEE International Workshops in Rapid System Prototyping (RSP 2001, 2002 & 2003),
- ◇ 3rd, 4th, 5th & 8th International Symposiums on Quality Electronic Design, (ISQED 2002, 2003, 2004 & 2007),
- ◇ 12th IEEE Mediterranean Electrotechnical Conference, 2004,
- ◇ International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS 2006, 2009, 2012 & 2014),
- ◇ 15th, 16th, 17th & 18th European Conference on Circuit Theory and Design, (ECCTD 2001, 2003, 2005 & 2007),
- ◇ 1st& 5th Asia Symposium on Quality Electronic Design, (ASQED 2009 & 2013),
- ◇ IEEE International Symposium on Circuits and Systems (ISCAS), 2009, 2010, 2012, 2014 & 2015,
- ◇ 18th IEEE/IFIP International Conference on VLSI and System-On-Chip (VLSI-SOC), 2010.

Άλλες δραστηριότητες

α. Συμμετοχή σε αναπτυξιακά / ερευνητικά προγράμματα

1. Ανάπτυξη ασύρματου ψηφιακού συστήματος οπτικής παρακολούθησης διεσπαρμένων τοπικά χώρων, Πρόγραμμα Ανάπτυξης Βιομηχανικής Έρευνας (ΠΑΒΕ), 1999, επιστημονικός υπεύθυνος.
2. Ανάπτυξη Αρχιτεκτονικής Βασισμένης σε Τεχνολογίες Java και Jini για την Διασφάλιση Επικοινωνιακής Ομογενοποίησης και Διαλειτουργικότητας Ετερογενών Βιομηχανικών Δικτύων Πεδίου (ΑΡΤΙΟ / JAVA-JINI ΣΤΗ ΒΙΟΜΗΧΑΝΙΑ), Πρόγραμμα Ενίσχυσης Ερευνητικού Δυναμικού, 1999, (ΠΕΝΕΔ '99), υπεύθυνος από πλευράς ομάδας του ΕΑΙΤΥ.
3. Ανάπτυξη μεθόδων για τον εύκολο έλεγχο ορθής λειτουργίας ολοκληρωμένων-συστημάτων σε πυρίτιο (System On Chip Testing), Πρόγραμμα Βασικής Έρευνας ¨Κ. Καραθεοδωρή¨, 2000, επιστημονικός υπεύθυνος.
4. Ανάπτυξη Επιχειρηματικότητας και Καινοτομίας στο Πανεπιστήμιο Πατρών, ΕΠΕΑΕΚ, Υποέργο 85978, 09/2002 – 03/2005, εξωτερικός συνεργάτης.
5. Ανάπτυξη μεθόδων σχεδιασμού και ελέγχου της ορθής λειτουργίας μονάδων επεξεργασίας δεδομένων για υλοποίηση σε τεχνολογίες πολύ μεγάλης κλίμακας ολοκλήρωσης, Πρόγραμμα Ενίσχυσης Ερευνητικών Ομάδων στα Πανεπιστήμια (ΠΥΘΑΓΟΡΑΣ), 2003, συνεργαζόμενο μέλος ΔΕΠ.
6. VLSI σχεδίαση και έλεγχος λειτουργικών βλαβών λειτουργικών μονάδων για επεξεργαστές σήματος (DSP) και συστήματα κρυπτογραφίας βασισμένα σε αριθμητικά συστήματα υπολοίπων, ΕΠΕΑΕΚ ΙΙ - ΑΡΧΙΜΗΔΗΣ ΙΙ : Πρόγραμμα Ενίσχυσης Ερευνητικών Ομάδων του ΤΕΙ Αθηνών, 2005, συνεργαζόμενο μέλος ΔΕΠ.
7. Ανάπτυξη Επιχειρηματικότητας και Καινοτομίας στο Πανεπιστήμιο Πατρών Φαση 2, ΕΠΕΑΕΚ, Υποέργο 99532, 15/09/2005 – 30/09/2008, εξωτερικός συνεργάτης.
8. Ανάπτυξη Τεχνικών Αύξησης της Αξιοπιστίας για Πολυπήρυνους Επεξεργαστές (HOLISTIC), Πρόγραμμα Θαλής 1103/2011, μέλος της ερευνητικής ομάδας.
9. Αντιμετώπιση Μόνιμων, Μεταβατικών & Διαλειπόντων Σφαλμάτων σε Νανομετρικά Ολοκληρωμένα Κυκλώματα-Συστήματα (REIN), Πρόγραμμα Θαλής 1217/2011, μέλος της ερευνητικής ομάδας.

β. Συμμετοχή σε διοργάνωση συνεδρίων

- ◇ Publicity Chair, 5th IEEE International On-Line Testing Workshop.
- ◇ Publications Chair, 6th IEEE International On-Line Testing Workshop.
- ◇ Publications Chair, 7th IEEE International On-Line Testing Workshop.

γ. Συμμετοχή σε εξεταστικές επιτροπές

Μέλος των εξεταστικών επιτροπών στις ακόλουθες μεταπτυχιακές διπλωματικές εργασίες :

- ◇ Ανάπτυξη εργαλείων για την αυτόματη παραγωγή και τον έλεγχο ορθής λειτουργίας αριθμητικών κυκλωμάτων, Μπακάλης Δημήτριος, ΠΜΣ / ΤΜΗΥΠ, Μάρτιος 2000.
- ◇ Ανάλυση και υλοποίηση αλγορίθμων για χωροθέτηση σε FPGAs, Σιμόπουλος Θεόδωρος, ΠΜΣ / ΤΜΗΥΠ, Σεπτέμβριος 2000.

◇ Εύκολα ελέγξιμοι κυψελλωτοί διαιρέτες, Σιδηρόπουλος Γεώργιος, ΠΜΣ / ΤΜΗΥΠ, Ιανουάριος 2001.

◇ Μία νέα αρχιτεκτονική αυτοελέγχου κυκλωμάτων βασισμένη σε ολισθητές γραμμικής ανάδρασης τροφοδοτούμενους από σημεία παρατήρησης, Μπέλλος Μάτσιεϊ, ΠΜΣ / ΤΜΗΥΠ, Αύγουστος 2001.

◇ Μία νέα τεχνική ομαδοποίησης διανυσμάτων ελέγχου για σχήματα παραγωγής διανυσμάτων δοκιμής βασισμένα σε ολισθητές γραμμικής ανάδρασης, Καλλίγερος Εμμανουήλ, ΠΜΣ / ΤΜΗΥΠ, Σεπτέμβριος 2001.

◇ Αναγνώριση προτύπου μετάδοσης σε συστήματα software radio, Κατσωνοπούλου Ιωάννα, ΠΜΣ / ΤΜΗΥΠ, Οκτώβριος 2002.

◇ Εργαλείο Επεξεργασίας και Γραφικής Απεικόνισης Ψηφιακών Κυκλωμάτων Περιγραφομένων σε Γλώσσα Υψηλού Επιπέδου, Παπαδόπουλος Δημήτριος, ΠΜΣ / ΤΜΗΥΠ, Μάρτιος 2003.

◇ Ανάπτυξη εργαλείων σχεδίασης και ελέγχου ορθής λειτουργίας κυκλωμάτων, Μαυρακάκης Ιωάννης, ΠΜΣ Ο.Σ.Υ.Λ., Ιούλιος 2006.

◇ Ασύρματοι Αισθητήρες και μικροελεγκτές, Μανωλόπουλος Χαράλαμπος, ΔΠΜΣ Η.Ε.Π., Νοέμβριος 2010.

Μέλος επταμελών εξεταστικών επιτροπών για τις διδακτορικές διατριβές :

◇ Σχεδίαση Αυτοελεγχόμενων Ελεγκτών, Χρυσοβαλάντης Καβουσιανός, Σεπτέμβριος 2000.

◇ Δομές ενσωματωμένου αυτοελέγχου για ψηφιακά κυκλώματα πολύ μεγάλης κλίμακας ολοκλήρωσης, Δημήτριος Μπακάλης, Οκτώβριος 2001.

◇ Τεχνικές Ενσωματωμένου Ελέγχου, Εμμανουήλ Καλλίγερος, Δεκέμβριος 2004.

◇ Τεχνικές ελέγχου ορθής λειτουργίας με έμφαση στη χαμηλή κατανάλωση ισχύος, Μάτσιεϊ Μπέλλος, Απρίλιος 2005.

◇ Μονάδες επεξεργασίας δεδομένων για μικροεπεξεργαστές υψηλών επιδόσεων, Γεώργιος Δημητρακόπουλος, Φεβρουάριος 2007.

◇ Αποδοτικά κυκλώματα για το Αριθμητικό Σύστημα Υπολοίπων, Ευάγγελος Βασσάλος, Μάρτιος 2013.

Κατόπιν επισήμων προσκλήσεων (επισυνάπτονται αντίγραφα στο Παράρτημα Ε) του Αναπληρωτή Καθηγητή κ. Chip Hong Chang (Αναπληρωτής Διευθυντής του Centre for High Performance Embedded Systems, διευθυντής προγράμματος του Centre for Integrated Circuits and Systems της Σχολής Ηλεκτρολόγων και Ηλεκτρονικών Μηχανικών στο Nanyang Technological University της Σιγκαπούρης και Associate Editor του IEEE Transactions on Circuits and Systems I) και κατόπιν κρίσης επί του βιογραφικού μου σημειώματος, διετέλεσα εξωτερικός κριτής :

◇ της μεταπτυχιακής διπλωματικής εργασίας του κ. Shibu Menon με τίτλο "Development of modulo adders, multipliers and shared-moduli architetctures for $\{2^n - 1, 2^n, 2^n + 1\}$ RNS", που ολοκληρώθηκε το Μάρτιο του 2007 και

◇ της διδακτορικής διατριβής του κ. J. Y. S. Low με τίτλο "VLSI Efficient RNS Scalers and Arbitrary Modulus Residue Generators" που ολοκληρώθηκε τον Ιούνιο του 2013.

δ. *Συμμετοχή στην ανοικτή και την εξ αποστάσεως εκπαίδευση*

- ◇ Κριτικός αναγνώστης του βιβλίου ¨Αρχιτεκτονική Υπολογιστών Ι¨ (συγγραφέας : Δ. Νικολός), της θεματικής ενότητας ¨Ψηφιακά Συστήματα¨, του προπτυχιακού προγράμματος σπουδών ¨Πληροφορική¨, του Ελληνικού Ανοικτού Πανεπιστημίου.
- ◇ Συνεργαζόμενο Εκπαιδευτικό Προσωπικό, της θεματικής ενότητας ¨Πληροφορική—21 : Ψηφιακά Συστήματα¨ κατά τα τελευταία 8 ακαδημαϊκά έτη.
- ◇ Ανάπτυξη εκπαιδευτικού υλικού (πάνω από 150 λυμμένες ασκήσεις σε θέματα Ψηφιακής Σχεδίασης καθώς και επιλεγμένες βιντεοδιαλέξεις) για εξ αποστάσεως εκαπίδευση. Το υλικό αυτό είνα διαθέσιμο μέσω της ιστοσελίδας μου.

ε. *Διοικητικό έργο και συμμετοχή σε επιτροπές*

- ◇ Επιτροπή αξιολόγησης προσφορών για τον διεθνή διαγωνισμό ΜΟΠ 10 του ΕΑΙΤΥ.
- ◇ Επιτροπή αξιολόγησης προσφορών για τον διεθνή διαγωνισμό ΜΟΠ 11 του ΕΑΙΤΥ.
- ◇ Επιτροπή μετεγγραφών του ΤΜΗΥΠ για τα ακαδημαϊκά έτη 1998–1999 έως και 2001–2002.
- ◇ Επιτροπή κατατακτηρίων εξετάσεων του ΤΜΗΥΠ από το ακαδημαϊκό έτος 1998–1999 έως σήμερα.
- ◇ Επιτροπή επιλογής μεταπτυχιακών φοιτητών για το ΠΜΣ / ΤΜΗΥΠ για το ακαδημαϊκό έτος 2000–2001
- ◇ Επιτροπή επιλογής μεταπτυχιακών φοιτητών για το ΠΜΣ ΟΣΥΛ (Ολοκληρωμένα Συστήματα Υλικού και Λογισμικού) από το ακαδημαϊκό έτος 1999–2000 έως σήμερα.
- ◇ Επιτροπή επιλογής μεταπτυχιακών φοιτητών για το ΔΠΜΣ ΗΕΠ (Ηλεκτρονική και Επεξεργασία της Πληροφορίας) από το ακαδημαϊκό έτος 2007–2008 έως σήμερα.
- ◇ Ειδική διατμηματική επιτροπή του ΠΜΣ ΣΕΣΕ (Συστήματα Επεξεργασίας Σημάτων και Εικόνων) κατά τα ακαδημαϊκά έτη 1998–1999 έως και 2006–2007.
- ◇ Ειδική διατμηματική επιτροπή του ΔΠΜΣ ΗΕΠ (Ηλεκτρονική και Επεξεργασία της Πληροφορίας) κατά τα ακαδημαϊκά έτη 2007–2008 έως σήμερα.
- ◇ Επιστημονική–Τεχνική επιτροπή του ΕΠΕΑΕΚ-ΠΜΣ του ΤΜΗΥΠ.
- ◇ Επιτροπή ΕΤΠΑ του ΤΜΗΥΠ για τη σύνταξη της προτάσεων αναβάθμισης του εξοπλισμού του, στα πλαίσια του ΕΠΕΑΕΚ ΙΙ.
- ◇ Επιτροπή επικοινωνίας με τους αποφοίτους του ΤΜΗΥΠ.
- ◇ Επιτροπή επαγγελματικών δικαιωμάτων του ΤΜΗΥΠ.
- ◇ Επιτροπή προβολής του ΤΜΗΥΠ.
- ◇ Επιτροπή αναγνώρισης μαθημάτων και αντιστοίχισης βαθμολογίας του ΤΜΗΥΠ.
- ◇ Επιτροπή διαγωνισμού του έργου ¨Συμπληρωματικός Εκπαιδευτικός Εξοπλισμός Τμημάτων του Πανεπιστημίου Πατρών - ΕΤΠΑ¨.
- ◇ Συντακτική επιτροπή της σειράς ΙΙΙ (Θέματα ΗΜ και Μηχανικού Η/Υ και Πληροφορικής) των Τεχνικών Χρονικών του ΤΕΕ (Παράρτημα ΣΤ).
- ◇ Εκπρόσωπος του ΤΜΗΥΠ στη Σύγκλητο από τη βαθμίδα του Λέκτορα κατά την ακαδημαϊκή χρονιά 2000–2001.
- ◇ Εκπρόσωπος του ΤΜΗΥΠ στον διεθνή οργανισμό Europractice, που έχει ως στόχο τη διάχυση σε ερευνητικά και ακαδημαϊκά Ιδρύματα των πλέον πρόσφατων τεχνολογιών μικροηλεκτρονικής, από το 1998 έως και το 2010.

◇ Διευθυντής του Τομέα Υλικού και Αρχιτεκτονικής των Υπολογιστών, κατά το ακαδημαϊκά έτη 2009–2010 και 2014–2015.

◇ Διευθυντής του Εργαστηρίου Ηλεκτρονικών Υπολογιστών (Υπολογιστικό Κέντρο), κατά το ακαδημαϊκό έτος 2011–2012 και κατά το εαρινό εξάμηνο του 2012–2013.

◇ Εξωτερικός εκλέκτορας για εκλογή σε βαθμίδα Επίκουρου Καθηγητή / Λέκτορα στο Τμήμα Ηλεκτρολόγων Μηχανικών & Μηχανικών Ηλεκτρονικών Υπολογιστών του Δημοκρίτειου Πανεπιστημίου Θράκης, με αντικείμενο ¨Σχεδιασμός Ολοκληρωμένων Κυκλωμάτων, Πολύ Μεγάλης Κλίμακας Ολοκλήρωσης¨, Ιανουάριος 2010.

◇ Μέλος της Εισηγητικής Επιτροπής για εκλογή στη βαθμίδα του Επίκουρου Καθηγητή, στο Τμήμα Πληροφορικής του Πανεπιστημίου Πειραιώς, με αντικείμενο ¨Αρχιτεκτονική Ενσωματωμένων Συστημάτων με Έμφαση στο Υλικό¨, Οκτώβριος 2010.

◇ Εξωτερικός εκλέκτορας για εκλογή σε βαθμίδα Επίκουρου Καθηγητή στο Τμήμα Ηλεκτρολόγων Μηχανικών & Μηχανικών Ηλεκτρονικών Υπολογιστών του Εθνικού Μετσοβείου Πολυτεχνείου, με αντικείμενο ¨Αυτοματοποιημένη Σχεδίαση Υλικού¨, Νοέμβριος 2010.

◇ Μέλος της Εισηγητικής Επιτροπής για τη μονιμοποίηση Επίκουρου Καθηγητή στο ΤΜΗΥΠ, ΠΠ, με αντικείμενο ¨Ηλεκτρονική με έμφαση στο Ψηφιακό Σχεδιασμό¨, Φεβρουάριος 2011.

◇ Μέλος της Εισηγητικής Επιτροπής για την πλήρωση θέσης Ειδικού Τεχνικού και Εκπαιδευτικού Προσωπικού (Ε.Τ.Ε.Π.) στο ΤΜΗΥΠ, ΠΠ, Φεβρουάριος 2011.

◇ Μέλος της Επιτροπής διενέργειας του διαγωνισμού για την προ•μήθεια του ενεργού και την εγκατάσταση του παθητικού δικτυακού εξοπλισμού για το νέο κτήριο του ΤΜΗΥΠ.

στ. Μέλος Συλλόγων και Επιμελητηρίων

◇ Institute of Electrical and Electronic Engineers (IEEE), Senior Member.

◇ Τεχνικό Επιμελητήριο Ελλάδος (ΤΕΕ).

◇ Ένωση Αποφοίτων Μηχανικών Η/Υ και Πληροφορικής Ελλάδος.

◇ Πανελλήνιος Σύλλογος Διπλωματούχων Μηχανικών Η/Υ και Πληροφορικής.

Παράρτημα Α.

ΠΑΝΕΠΙΣΤΗΜΙΟ ΠΑΤΡΩΝ
ΠΟΛΥΤΕΧΝΙΚΗ ΣΧΟΛΗ
ΤΜΗΜΑ ΜΗΧΑΝΙΚΩΝ
ΗΛΕΚΤΡΟΝΙΚΩΝ ΥΠΟΛΟΓΙΣΤΩΝ
ΚΑΙ ΠΛΗΡΟΦΟΡΙΚΗΣ
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UNIVERSITY OF PATRAS
SCHOOL OF ENGINEERING
DEPARTMENT OF
COMPUTER ENGINEERING AND INFORMATICS
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ΤΟΜΕΑΣ ΥΛΙΚΟΥ ΚΑΙ ΑΡΧΙΤΕΚΤΟΝΙΚΗΣ ΤΩΝ ΥΠΟΛΟΓΙΣΤΩΝ

ΤΗΛΕΦΩΝΑ : (061) 997-572
997-642
FAX : 991-909

Πάτρα 11-3-1996
Αριθμ. Πρωτ. : -89-

Προς: τη Γενική Συνέλευση του Τμήματος

Η Γενική Συνέλευση 13/28.2.1996 του Τομέα Υλικού και Αρχιτεκτονικής των Υπολογιστών, αποφάσισε ομόφωνα την ανάθεση του μαθήματος "Συστήματα Υπολογιστών Π" του εκλιπόντος συναδέλφου Αν. Βέργη, στον διδάκτορα του τμήματος, κ. Χ. Βέργο με υπεύθυνο επιβλέποντα τον κ. Γ. Αλεξίου. Η λύση αυτή προτείνεται μόνο για την τρέχουσα ακαδημαϊκή χρονιά 1995-96.

Η Γενική Συνέλευση του Τομέα Υλικού και Αρχιτεκτονικής των Υπολογιστών, ζητά από το τμήμα να μεριμνήσει για την διεκδίκηση και προκήρυξη νέων θέσεων μελών ΔΕΠ για τον τομέα. Ο τομέας προσφέρει περισσότερο από το 50% των υποχρεωτικών μαθημάτων του Προγράμματος Σπουδών του τμήματος και όμως διαθέτει μόλις το 30% του αριθμού των μελών ΔΕΠ.

Αυτή τη στιγμή σημαντικό μέρος μαθημάτων του τομέα ή δεν γίνονται καθόλου (π.χ. ΣΑΕ, Τηλεπικοινωνίες, Στοχαστικά Σήματα) ή "υπολειτουργούν" (π.χ. Εργαστήρια Μικροϋπολογιστών).

Ο τομέας ζητά από τους άλλους δύο τομείς να διαθέσουν μικρό αριθμό από μεταπτυχιακούς φοιτητές για να συνεπικουρήσουν στην διεξαγωγή βασικών εργαστηρίων του Α', Β' και Γ' έτους (Assembly, Λογικού Σχεδιασμού, Ηλεκτρονικών, Αρχιτεκτονικής, Μικροϋπολογιστών).

Ο ΔΙΕΥΘΥΝΤΗΣ ΤΟΥ ΤΟΜΕΑ

Γ. ΑΛΕΞΙΟΥ
ΑΝΑΠΛ. ΚΑΘΗΓΗΤΗΣ

JSA **Journal of Systems Architecture**
The EUROMICRO Journal

Milano, January 20, 1996

Prof. H.T. Vergos et al.
School of Engineering
Dept. of Computer Eng. & Informatics
26500 Patras - Greece

Ref. Paper JSA-017
Reconfigurable CPU Cache Memory Design: Fault Tolerance and Performance Evaluation

Dear prof. Vergos,
please find enclosed comments on the paper above. Reviewers judged your paper publishable, but it needs major modifications, although they think it is an excellent paper.
Please check the reviews carefully, revisioning the paper. I am sure you understand that what I'm asking for is **a major** revision of it.
If you feel you can respond to the objections raised by reviewers, I'd like to encourage you to revise the paper. In such a case, I would appreciate receiving a written description of how you dealt with the reviews, and I would be happy to send out the revised paper and letter to the reviewers, asking for a second revision.

As you can notice from this headed letter, we have changed the name of our Journal: scopes and aims are the same as before.

Waiting for the revised version of the paper, I remain

Yours sincerely,

Enza Caputo

Reply to the marked address:

Editor in chief:
❑ Prof. Mariagiovanna Sami
Politecnico di Milano
Dip. Elettronica e Informazione
Piazza Leonardo da Vinci 32
I 20133 Milano – Italy
Phone: +39 – 2 – 2399 3516
Fax: +39 – 2 – 2399 3411
e-mail: sami@elet.polimi.it

Editor in chief:
❑ Prof. Lutz Richter
Universität Zürich
Institut für Informatik
Winterthurerstr, 190
CH 8057 Zürich – Switzerland
Phone: +41 – 1 – 257 4330/1
Fax: +41 – 1 – 363 0035
e-mail: richter@ifi.unizh.ch

Editorial Office:
❑ Ms. Enza Caputo
Politecnico di Milano
Dip. Elettronica e Informazione
Piazza Leonardo da Vinci 32
I 20133 Milano – Italy
Phone: +39 – 2 – 2399 3405
Fax: +39 – 2 – 2399 3411
e-mail: caputo@elet.polimi.it

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Παράρτημα Δ. Κατάλογος ετεροαναφορών

α. Από τρίτους

α.1. Ευρεσιτεχνίες

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T.4. Residue Number Systems: Algorithms and Architectures, P. V. Ananda Mohan, Kluwer Academic Publishers, 2002.

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T.7. Residue Number Systems Theory and Implementation, A. Omondi and B. Premkumar, Imperial College Press, 2007.

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T.9. Computer Arithmetic : Algorithms and Hardware Implementations, Mircea Vlădutiu, Springer-Verlag 2012, ISBN : 978-3-642-18314-0.

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T.11. Σχεδίαση Αυτοελεγχόμενων Ελεγκτών σε Τεχνολογία VLSI, Χ. Καβουσιανός, Διδακτορική Διατριβή, Τμήμα Μηχανικών Η/Υ και Πληροφορικής, Πανεπιστήμιο Πατρών, Σεπτέμβριος 2000.

T.12. Power Minimization Techniques for Testing Low Power VLSI Circuits, N. Nicolici, Ph.D. Thesis, University of Southampton, October 2000.

T.13. Fault–Tolerant Computing for Radiation Environments, P. P. Shirvani, Ph.D. Thesis, Department of Electrical Engineering and Computer Science, Stanford University, July 2001.

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T.17. Modelo Paramétrico de Arquitectura para la Generación de Primitivas Computacionales, M. T. S. Pont, Departamento de Tecnología Informática y Computación, Universidad de Alicante, May 2005.

T.18. An Energy Efficient 32–bit Multiplier Architecture in 90–nm CMOS, N. Mehmood, M.Sc. Thesis, Linköping Institute of Technology, Electronic Devices Division, September 2006.

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T.25. Efficient Parallel Prefix Algorithms on the Multicomputer and Circuit Models, Li–Ling Hung, Ph. D. Thesis, Department of Computer Science and Information Engineering, National Twaivan University of Science and Tecnology, 24 July 2008.

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T.32. Improved Parallel Prefix on the Multicomputer, J.–Y. Ke, Master of Science Thesis, National Taiwan University of Science and Technology, Department of Computer Science and Information Engineering, September 2009.

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T.38. Built–in Self Test for Digital Signal Processor Cores in Virtex–4 and Virtex–5 Field Programmable Gate Arrays, M. D. Pulukuri, Master of Science Thesis, Auburn University, Alabama, August 2010.

T.39. Analysis and Design of High Performance 128–bit Parallel–Prefix End–Around–Carry Adder, O. Turkyilmaz, Master of Science Thesis, Northeastern University, Dept. of Electrical and Computer Engineering, 2011.

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T.41. Research and Implementation of Area/Delay–Efficient Modulo $2^n + 1$ Adders, C.–C. Chiu, Master of Science Thesis, Department of Computer Science and Information Engineering, National Pingtung Institute of Commerce, Taiwan, R.O.C., April 2011.

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α.5. Δημοσιεύματα σε συλλογές άρθρων ή συνέδρια τα πρακτικά των οποίων εκδόθηκαν σαν βιβλία

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Οι αναφορές των πιο πάνω εργασιών στο ερευνητικό μου έργο συνοψίζονται στους επόμενους πίνακες :

Αναφερόμενη Εργασία	*Αναφέρουσες Εργασίες*	*Αναφορές από τρίτους*	*Αναφορές από συσυγγραφείς*
J.1	T.1, T.2, T.11, T.65, T.110, T.129, T.161, T.200, T.267, T.274, T.285, T.332, T.376, T.387, T.398, T.406, T.408, T.409, T.410,	16	3
J.2	T.56, T.80, T.98, T.99, T.239, T.256, T.293,	7	
J.3	T.4, T.7, T.17, T.20, T.21, T.28, T.29, T.30, T.31, T.37, T.39, T.47, T.50, T.51, T.55, T.57, T.58, T.59, T.66, T.67, T.68, T.69, T.70, T.71, T.74, T.76, T.79, T.82, T.86, T.87, T.92, T.94, T.95, T.105, T.106, T.112, T.115, T.118, T.122, T.124, T.132, T.135, T.136, T.141, T.151, T.154, T.157, T.158, T.172, T.174, T.178, T.184, T.186, T.190, T.198, T.199, T.207, T.215, T.216, T.217, T.231, T.234, T.236, T.240, T.242, T.261, T.262, T.264, T.265, T.266, T.269, T.270, T.278, T.283, T.288, T.290, T.296, T.299, T.302, T.303, T.304, T.307, T.313, T.314, T.318, T.319, T.338, T.341, T.357, T.358, T.368, T.374, T.383, T.388, T.390, T.392, T.397, T.403, T.429,	98	1
J.5	T.148,	1	
J.6	T.237, T.294,	2	
J.7	T.9, T.21, T.28, T.30, T.31, T.34, T.35, T.36, T.41, T.45, T.47, T.48, T.49, T.50, T.51, T.52, T.70, T.76, T.78, T.85, T.90, T.91, T.95, T.100, T.111, T.114, T.117, T.125, T.128, T.130, T.133, T.136, T.137, T.139, T.141, T.142, T.144, T.149, T.158, T.160, T.162, T.166, T.169, T.172, T.174, T.178, T.181, T.183, T.186, T.189, T.190, T.192, T.193, T.195, T.196, T.201, T.203, T.211, T.216, T.220, T.223, T.233, T.234, T.238, T.263, T.264, T.279, T.281, T.282, T.287, T.290, T.298, T.300, T.301, T.304, T.305, T.309, T.312, T.317, T.318, T.320, T.321, T.322, T.324, T.325, T.327, T.329, T.330, T.333, T.338, T.339, T.343, T.349, T.354, T.355, T.365, T.370, T.372, T.375, T.379, T.381, T.386, T.389, T.397, T.417, T.419, T.421, T.422, T.427,	99	10
J.8	T.50, T.90, T.117, T.141, T.164, T.166, T.236, T.242, T.327, T.329, T.338, T.350, T.361, T.417, T.419, T.421, T.422, T.428,	10	8
J.9	T.143, T.407,	2	
J.10	T.9, T.28, T.30, T.33, T.35, T.39, T.41, T.49, T.61, T.74, T.76, T.82, T.87, T.91, T.95, T.114, T.130, T.139, T.145, T.152, T.166, T.172, T.186, T.189, T.193, T.196, T.207, T.209, T.210, T.220, T.223, T.243, T.245, T.246, T.265, T.281, T.287, T.289, T.299, T.306, T.309, T.317, T.319, T.322, T.328, T.329, T.333, T.338, T.339, T.342, T.343, T.370, T.371, T.390, T.392, T.397, T.417, T.419, T.421,	53	6
J.11	T.22, T.23, T.24, T.31, T.47, T.50, T.60, T.66, T.67, T.68, T.69, T.70, T.72, T.74, T.82, T.103, T.108, T.113, T.116, T.117, T.122, T.125, T.134, T.138, T.140, T.151, T.158, T.170, T.171, T.173, T.174, T.178, T.179, T.190, T.198, T.202, T.208, T.213, T.216, T.221, T.224, T.234, T.242, T.247, T.248, T.260, T.266, T.268, T.283, T.295, T.314, T.318, T.319, T.357, T.358, T.374, T.426,	56	1
J.12	T.7, T.25, T.27, T.28, T.32, T.47, T.49, T.51, T.64, T.75, T.76, T.78, T.85, T.86, T.88, T.89, T.90, T.93, T.95, T.97, T.101, T.106, T.107, T.115, T.118, T.122, T.123, T.126, T.127, T.132, T.135, T.136, T.159, T.163, T.165, T.166, T.168, T.172, T.188, T.191, T.193, T.199, T.204, T.208, T.217, T.221, T.222, T.227, T.241, T.271, T.273, T.279, T.288, T.291, T.302, T.304, T.308, T.313, T.325, T.327, T.329, T.337, T.338, T.340, T.341, T.375, T.379, T.397, T.399, T.400, T.401, T.402, T.403, T.405, T.417, T.419, T.421, T.422,	70	8
J.13	T.21, T.24, T.35, T.36, T.47, T.50, T.70, T.76, T.108, T.111, T.117, T.119, T.120, T.121, T.133, T.137, T.144, T.149, T.150, T.158, T.160, T.162, T.164, T.168, T.169, T.174, T.178, T.179, T.185, T.186, T.190, T.203, T.236, T.245, T.246, T.276, T.297, T.298, T.300, T.301, T.304, T.305, T.311, T.316, T.321, T.322, T.324, T.327, T.328, T.329, T.330, T.334, T.347, T.348, T.350, T.354, T.361, T.369, T.370, T.371, T.382, T.417, T.419, T.421, T.422, T.428,	59	7
J.14	T.31, T.48, T.190, T.280, T.298, T.359, T.372,	7	
J.15	T.50, T.123, T.188, T.191, T.222,	5	
J.16	T.40, T.44, T.102, T.310, T.377, T.380, T.391, T.393, T.404,	9	
J.17	T.190, T.242,	2	
J.18	T.36, T.45, T.48, T.50, T.51, T.104, T.111, T.116, T.117, T.122, T.129, T.133, T.134, T.144, T.146, T.147, T.149, T.150, T.156, T.158, T.166, T.168, T.174, T.178, T.179, T.185, T.190, T.196, T.202, T.297, T.298, T.300, T.316, T.317, T.321, T.323, T.341, T.347, T.352, T.354, T.357, T.372, T.375, T.416, T.420, T.422, T.423, T.428,	40	8

Αναφερόμενη Εργασία	*Αναφέρουσες Εργασίες*	*Αναφορές από τρίτους*	*Αναφορές από συσυγγραφείς*
J.19	T.8, T.41, T.111, T.114, T.117, T.124, T.133, T.139, T.163, T.164, T.166, T.172, T.186, T.188, T.189, T.191, T.192, T.193, T.194, T.195, T.198, T.201, T.206, T.220, T.222, T.223, T.241, T.324, T.327, T.329, T.333, T.336, T.364, T.365, T.375, T.417, T.421, T.422, T.428,	31	8
J.20	T.49, T.50, T.130, T.141, T.184, T.242, T.334, T.417,	5	3
J.21	T.28, T.43, T.48, T.49, T.51, T.131, T.158, T.163. T.166, T.167, T.178, T.193, T.196, T.211, T.232, T.235, T.241, T.318, T.338, T.341, T.353, T.359, T.370, T.375, T.421, T.422, T.424, T.428,	20	8
J.22	T.49, T.50, T.119, T.130, T.338, T.353, T.363,	5	2
J.23	T.50, T.141, T.197, T.357,	3	1
J.24	T.50, T.214, T.242, T.357,	2	2
J.25	T.50, T.242, T.353,		3
J.26	T.50, T.182, T.186, T.193, T.196, T.199, T.211, T.212, T.220, T.236, T.353, T.365, T.369, T.370, T.375,	15	
J.27	T.50, T.176, T.190,	3	
J.29	T.384,	1	
B.2	T.292,	1	
I.1	T.50,		1
C.1	T.1, T.2, T.6, T.13, T.26, T.62, T.65, T.244, T.249, T.267, T.286, T.292, T.387, T.395, T.396, T.398, T.425, T.427, T.430,	16	3
C.2	T.19, T.80,	2	
C.4	T.10, T.43, T.53, T.250, T.251, T.385,	6	
C.5	T.257,	1	
C.7	T.272,	1	
C.9	T.3, T.12, T.177, T.228, T.237,	5	
C.10	T.73, T.255,	2	
C.11	T.5, T.14, T.18, T.38, T.63, T.259, T.315, T.331, T.394, T.411,	9	1
C.14	T.51, T.77, T.96, T.131, T.254, T.258, T.354, T.426, T.429,	7	2
C.15	T.83, T.274, T.412, T.413, T.415,	2	3
C.16	T.29, T.33, T.34, T.85, T.164, T.252, T.253, T.277, T.279, T.350, T.361, T.397,	12	
C.17	T.27, T.42, T.53, T.312,	4	
C.18	T.76, T.85, T.95, T.279, T.284,	5	
C.19	T.15, T.16, T.218, T.225, T.326, T.346, T.360, T.414, T.416, T.420, T.424,	7	4
C.20	T.392,	1	
C.21	T.20, T.74, T.82,	2	1
C.23	T.20, T.74, T.81, T.82, T.212, T.226, T.296, T.327, T.386, T.426,	7	3
C.24	T.84, T.109, T.143, T.153, T.378,	5	
C.26	T.35, T.47, T.317,	3	
C.29	T.20, T.49, T.124, T.130, T.136, T.151, T.157, T.158, T.170, T.178, T.198, T.229, T.307, T.314, T.317, T.318, T.319, T.335, T.358, T.362, T.367, T.426, T.429,	20	3
C.30	T.168, T.324,	2	
C.31	T.31,	1	
C.32	T.230, T.344, T.366,	3	
C.34	T.126, T.175, T.180, T.217, T.356,	5	
C.35	T.41, T.114, T.136, T.139, T.189, T.192, T.194, T.213, T.223, T.241, T.330, T.333,	12	
C.37	T.50, T.51, T.327, T.329,	3	1
C.39	T.50,		1
C.40	T.190, T.224, T.345,	3	
C.41	T.166, T.191,	2	
C.42	T.351, T.353, T.363,	3	
C.43	T.50,		1
C.44	T.50, T.188, T.191, T.222,	3	1
C.45	T.50, T.190,	1	1
C.48	T.50,		1
C.49	T.50, T.219,	1	1

Παράρτημα Ε.

Centre for High Performance Embedded Systems

Dr. Chip Hong Chang
Deputy Director, Centre for High Performance Embedded Systems
Program Director, Centre for Integrated Circuits and Systems
Associate Professor, School of Electrical and Electronic Engineering
Nanyang Technological University, Singapore

28 December 2006

Professor Haridimos T. Vergos
Computer Architecture & Technology Lab
Dept. of Computer Engineering & Informatics
Patras University, 26 500,
Rio Greece

Dear Professor Vergos,

Re: External Examiner of Master of Engineering Thesis

I would like to invite you to be the external examiner of Mr. Shibu Menon's Master of Engineering thesis. The topic of his thesis is "Development of modulo adders and multipliers for $\{2^n-1, 2^n, 2^n+1\}$ RNS" and it is planned to be submitted in early January 2007. You are a highly regarded expert in this field and I would be glad if you could act as Mr. Shibu Menon's thesis examiner.

Thank you.

Sincerely yours,

50, Nanyang Drive, Research TechnoPlaza, 3rd Story, BorderX Blk, Singapore 637553
Tel: 65-67905873 Fax: 65-67920415 E-mail: echchang@ntu.edu.sg

NANYANG TECHNOLOGICAL UNIVERSITY

Graduate Studies Office

Reg. No. 200604393R

Ref: P/f

8 June, 2007

Professor Chardimos Theofanis Vergos
Department of Computer Engineering & Informatics
University of Patras
26500 Rio
Greece

Dear Professor Chardimos Theofanis Vergos

We would like to thank you for examining the thesis of our following Master of Engineering student:

Student's Name:	Shibu Menon
Degree of Study:	Master of Engineering
Commencement Date:	14 January 2003
School:	Electrical and Electronic Engineering
Division:	Circuits & Systems
Thesis Title:	Modulo Adders, Multipliers and Shared-Moduli Architectures for Moduli of Type {2n-1, 2n, 2n+1}

We have received your thesis examination report on 27 April 2007.

Thank you.

Yours sincerely,

NANYANG TECHNOLOGICAL UNIVERSITY GRADUATE STUDIES OFFICE

Chan Siew Mui
for DEAN, GRADUATE STUDIES

42 Nanyang Avenue, Student Services Centre Level 3, Singapore 639815
Tel: (65) 6790 6075 Fax: (65) 6793 1140
E-mail: gradstudies@ntu.edu.sg Website: www.ntu.edu.sg

NANYANG TECHNOLOGICAL UNIVERSITY

Graduate Studies Office

Reg No. 200604393R

Ref: P/F

01 July 2013

ASSOC PROF HARIDIMOS VERGOS
UNIV OF PATRAS
COMPUTER ENGG & INFORMATICS DEPT
26 500 RIO GREECE

Dear ASSOC PROF HARIDIMOS VERGOS

Ph.D. (EEE)
Candidate - JEREMY LOW YUNG SHERN

Thank you for agreeing to be the external examiner for the abovenamed candidate.

Enclosed are copies of the following:

(i) Thesis entitled "VLSI Efficient RNS Scalers and Arbitrary Modulus Residue Generators"
(ii) Instructions to Examiners
(iii) Form for Confidential Report of Examiner

Please complete the examination of the thesis and submit your report within two months from the date of this letter. The examiner's fee is US$500. Should there be remarks made on the examined thesis (see para 2 of the Instructions to Examiners), please return it to us together with your report. Kindly let us know the postage (in US$) you incurred in sending back the thesis by second class airmail so that we can reimburse you for the postage and include the sum in the payment of examiner's fee.

Please acknowledge your receipt of the thesis via email to Thesis-Research@ntu.edu.sg upon receiving the thesis. Thank you.

Yours sincerely,

Chan Nai Hong (Mdm)
for Associate Provost (Graduate Education)

cc Chair, EEE

42 Nanyang Avenue, Student Services Centre Level 3, Singapore 639815.
Tel: (65) 6790 5895 / 6790 4079 / 6790 4704 Fax: (65) 6793 1140
E-mail: gradstudies@ntu.edu.sg Website: www.ntu.edu.sg

Παράρτημα ΣΤ.

ΕΛΛΗΝΙΚΗ ΔΗΜΟΚΡΑΤΙΑ

ΤΕΧΝΙΚΟ ΕΠΙΜΕΛΗΤΗΡΙΟ ΕΛΛΑΔΑΣ

ΚΑΡΑΓΕΩΡΓΗ ΣΕΡΒΙΑΣ 4, 105 62 - ΤΗΛ. 32 54 590 - 9

TELEX 218374 - TELEFAX 3221772

Αθήνα, 16-7- 2003

ΤΜΗΜΑ ΕΚΔΟΣΕΩΝ

Πληροφορίες Π. Καζάζη τηλ. (210) 3671183 fax: 3618609

Αριθ. πρωτ. 1478

Π ρ ο ς
τον κ. Χαρίδημο Βέργο
Λέκτορα Πανεπιστημίου Πατρών
Πολυτεχνική Σχολή
Τμήμα Μηχανικών Η/Υ και Πληροφορικής
Τομέα Υλικού και Αρχιτεκτονικής Η/Υ
Εργαστήριο Τεχνολογίας Υλικού και Αρχιτεκτονικής
265 00 ΠΑΤΡΑ

Αγαπητέ συνάδελφε,

Θα θέλαμε να σας ευχαριστήσουμε για την πολυετή προσφορά σας ως μέλους της Συντακτικής Επιτροπής της Επιστημονικής Έκδοσης των Τεχνικών Χρονικών, Σειράς ΙΙΙ (Θέματα Ηλεκτρολόγου Μηχανικού και Μηχανικού Η/Υ και Πληροφορικής) και την αναμφισβήτητη συμβολή σας στη δύσκολη προσπάθεια αναβάθμισης του περιοδικού.

Η επικοινωνία που είχαμε μαζί σας το χρονικό αυτό διάστημα ήταν άριστη και θέλουμε να ελπίζουμε σε μια νέα συνεργασία μαζί σας.

Με εκτίμηση
Ο Πρόεδρος

Γιάννης Αλαβάνος